

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- Surface-mounted package
- Low gate charge

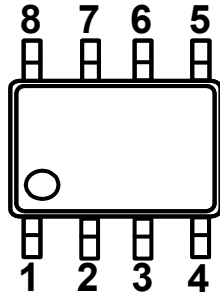
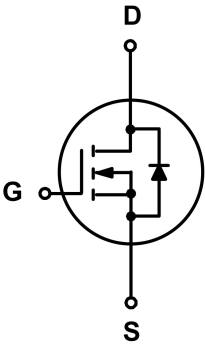
1.2 Applications

- Motor driver appliances
- High power inverter system
- Adapter appliances

1.3 Quick reference

- $BV \geq 40\text{ V}$
- $R_{DS(ON)} \leq 10\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- $P_{tot} \cong 2\text{ W}$
- $R_{DS(ON)} \leq 15\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- $I_D \cong 11\text{ A}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source	 Top View SOP- 8L	
4	Gate		
5,6,7,8	Drain		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	Drain-Source Voltage	T _A = 25 °C	40	-	V
V _{GS}	Gate-Source Voltage	T _A = 25 °C	-	± 20	V
I _D *	Drain Current	T _A = 25 °C, V _{GS} = 10 V	-	11	A
I _{DM} *	Pulsed Drain Current	T _A = 25 °C, V _{GS} = 10 V	-	44	A
P _{tot} *	Total Power Dissipation	T _A = 25 °C	-	2	W
T _{stg}	Storage Temperature		- 55	150	°C
T _J	Junction Temperature		-	150	°C
R _{θJC} *	Thermal Resistance- Junction to Case		-	3.5	°C / W
R _{θJA} *	Thermal Resistance- Junction to Ambient		-	62.5	°C / W

Notes :

- * Surface Mounted on 1 in² pad area, t ≤ 10 sec
- ** Pulse width ≤ 10 μs, duty cycle ≤ 1 %
- *** limited by bonding wire

4. Marking Information

Product Name	Marking
KJ4010S	<div style="display: inline-block; background-color: black; color: white; padding: 2px;">4010 YWWXXX</div> YWWXXX: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
KJ4010S	SOP8			3000	

Note: KUAJIEXIN defines “ Green ” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

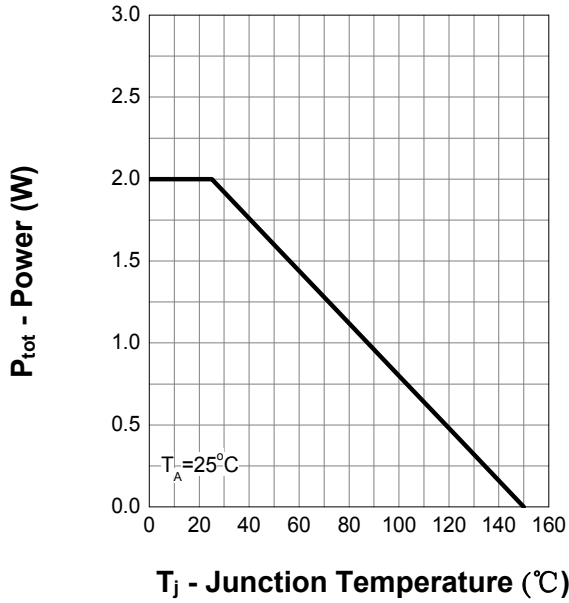
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\text{ }\mu\text{A}$	40	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\text{ }\mu\text{A}$	1.0	-	2.0	V
I_{DSS}	Drain Leakage Current	$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA
$R_{DS(ON)}^a$	Channel On-State Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	8.5	10	m Ω
	Channel On-State Resistance	$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	-	12	15	
Diode Characteristics						
V_{SD}^a	Diode Forward Voltage	$I_{SD} = 10\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 10\text{ A}, dI_{SD} / dt = 100\text{ A} / \mu\text{s}$	-	10	-	nS
Q_{rr}	Reverse Recovery Charge		-	4	-	nC
Dynamic Characteristics^b						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ Frequency = 1 MHz	-	1628	-	pF
C_{oss}	Output Capacitance		-	112	-	
C_{rss}	Reverse Transfer Capacitance		-	87	-	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = 20\text{ V}, V_{GEN} = 10\text{ V},$ $R_G = 4.5\text{ }\Omega, R_L = 2\text{ }\Omega,$ $I_{DS} = 10\text{ A}$	-	6.4	-	nS
t_r	Turn-on Rise Time		-	26	-	
$t_d(off)$	Turn-off Delay Time		-	34	-	
t_f	Turn-off Fall Time		-	25	-	
Gate Charge Characteristics^b						
Q_g	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V},$ $I_{DS} = 10\text{ A}$	-	30	-	nC
Q_{gs}	Gate-Source Charge		-	6	-	
Q_{gd}	Gate-Drain Charge		-	4.5	-	

Notes :

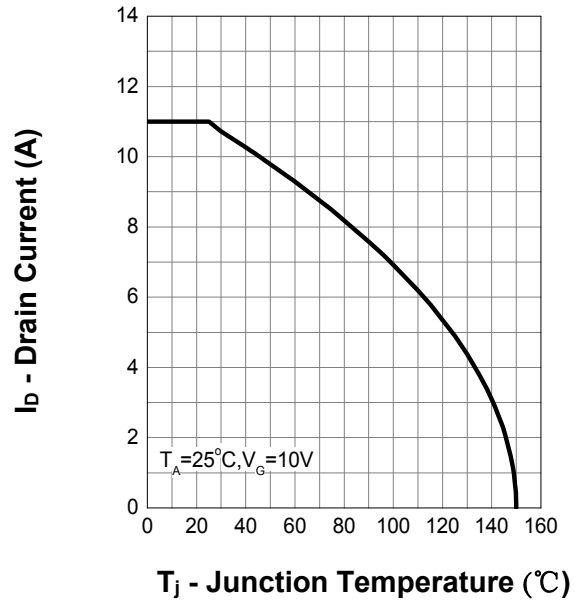
- a : Pulse test ; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
 b : Guaranteed by design, not subject to production testing

7. Typical Characteristics

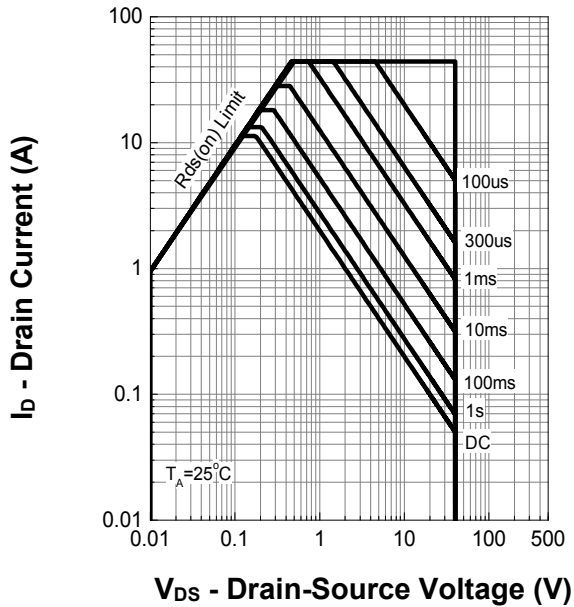
Power Dissipation



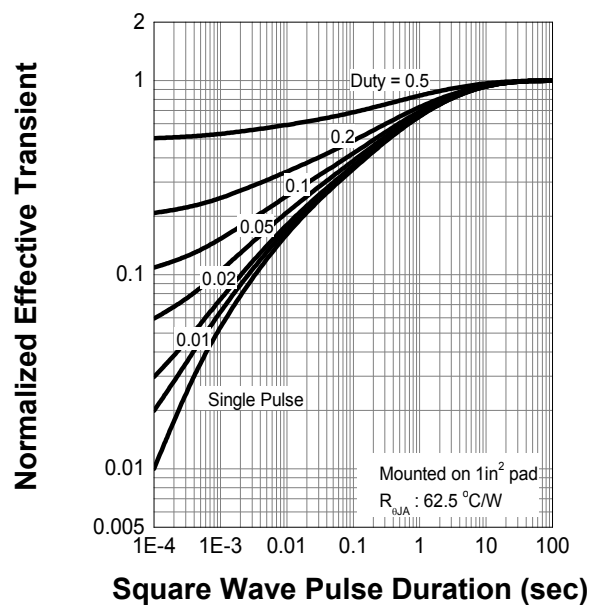
Drain Current



Safe Operation Area

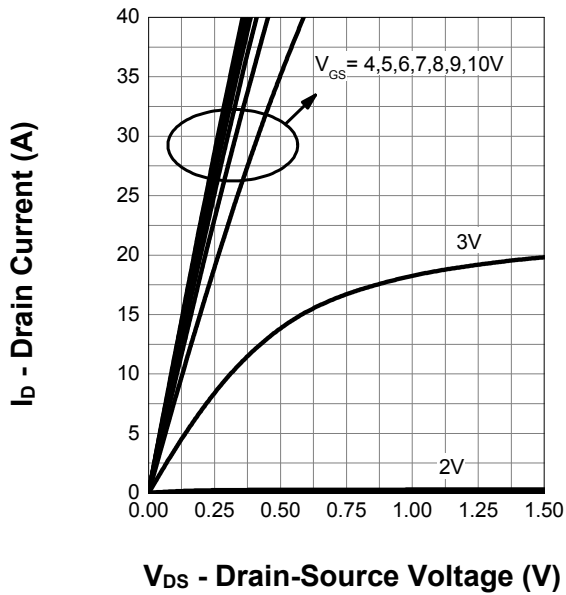


Thermal Transient Impedance

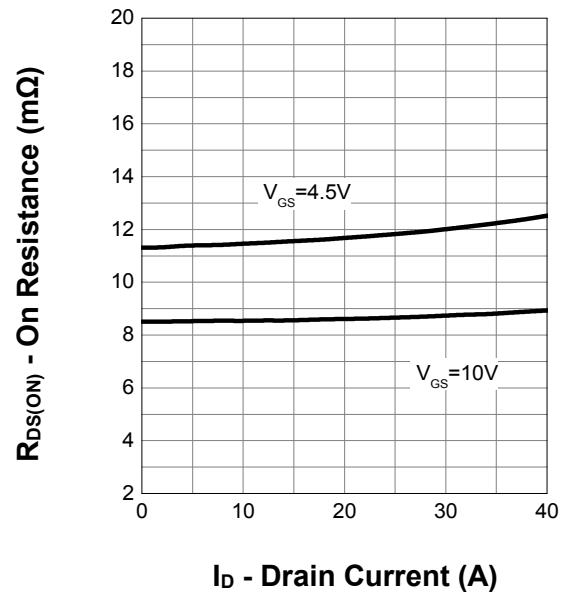


7. Typical Characteristics (cont.)

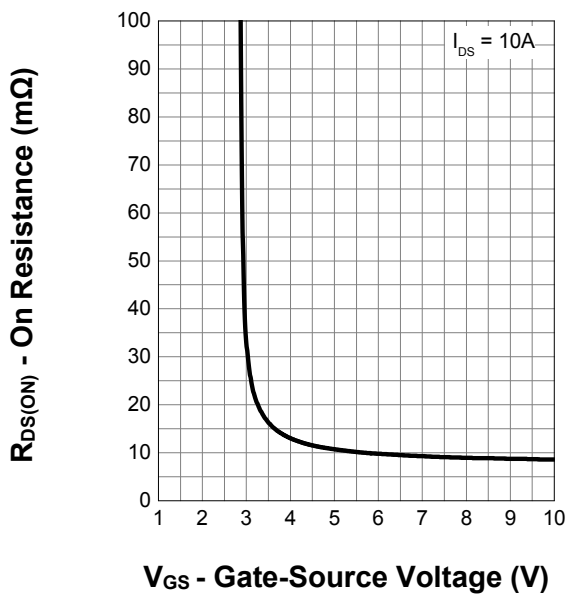
Output Characteristics



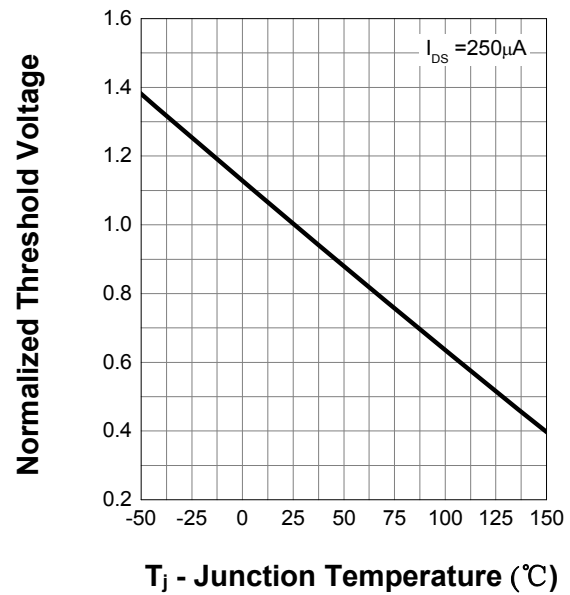
Drain-Source On Resistance



Transfer Characteristics

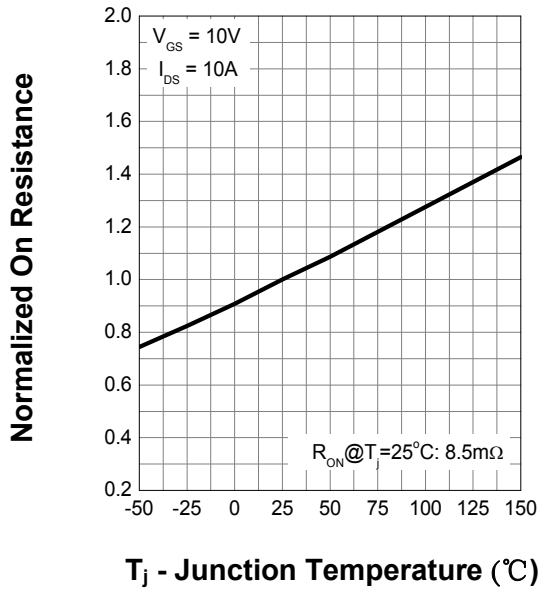


Gate Threshold Voltage

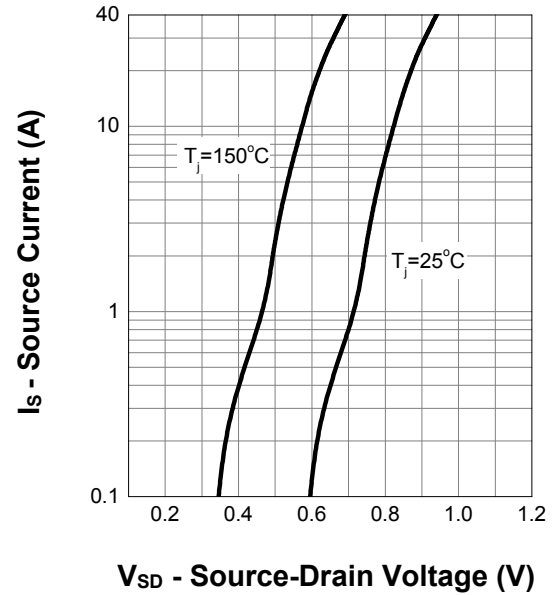


7. Typical Characteristics (cont.)

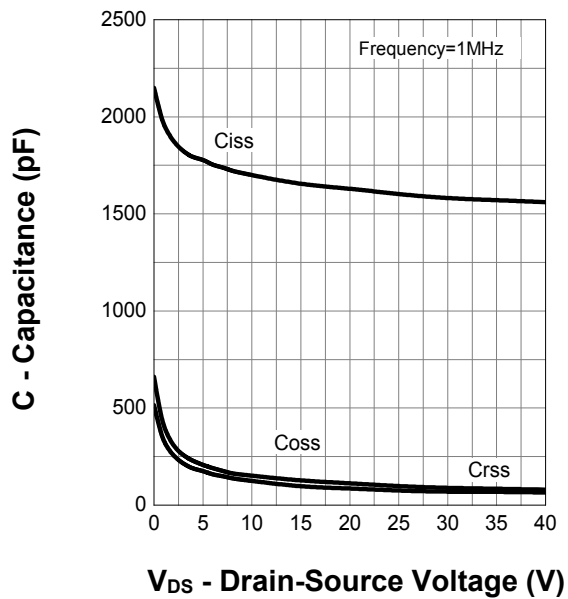
Drain-Source On Resistance



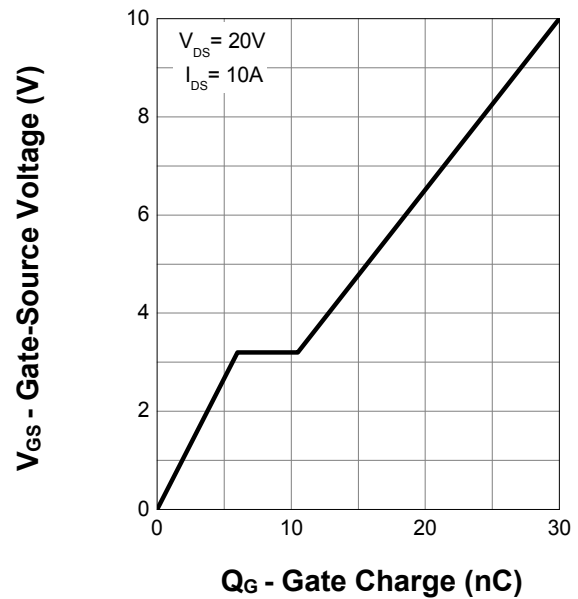
Source-Drain Diode Forward



Capacitance

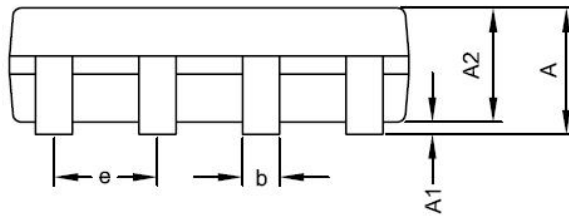
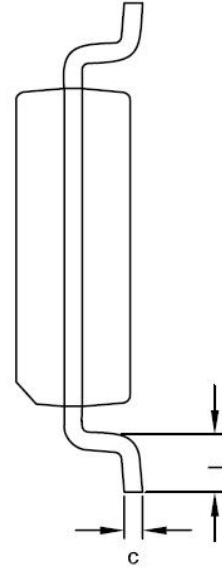
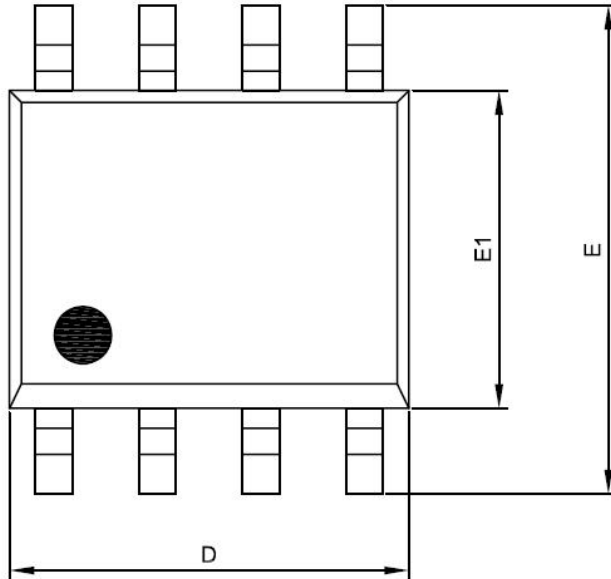


Gate Charge



8. Package Dimensions

SOP-8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

1. Jedec outline : MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.